IN THE CLAIMS

1 (Original). A method comprising:

machining a hole on an integrated circuit with a scanning probe system; and

performing a circuit edit through the hole formed by said system.

2 (Original). The method of claim 1 including machining said hole on the backside of the integrated circuit.

3 (Original). The method of claim 2 including machining a hole as a series of progressively smaller trenches through the backside of a silicon wafer.

4 (Original). The method of claim 1 including providing an electrical connection between said integrated circuit and said tool.

5 (Original). The method of claim 3 including detecting an open circuit when the tool reaches an isolation region.

6 (Original). The method of claim 3 including detecting a short circuit when the tool reaches a metallization.

7 (Original). The method of claim 1 including covering a portion of said hole with an insulating layer.

8 (Original). The method of claim 7 including covering said hole with an insulating layer before exposing a metallization.

9 (Original). The method of claim 1 including spring biasing a cantilever of an atomic force microscopy tool against an integrated circuit.

10 (Original). A method comprising:

forming a first trench having sidewalls and a bottom in a semiconductor structure using a scanning probe system;

forming a second trench through said bottom, said second trench having sidewalls that are spaced more closely than the sidewalls of said first trench; and

using said trench to perform a circuit edit.

11 (Original). The method of claim 10 including biasing an atomic force microscopy tip against the semiconductor surface to move atomic layers to form said trenches.

12 (Original). The method of claim 11 providing an electrical connection between said semiconductor structure and said tip.

13 (Original). The method of claim 12 including detecting an open circuit when said tip reaches an isolation region in said semiconductor structure.

14 (Original). The method of claim 12 including detecting a short circuit once the tip reaches a metallization in said semiconductor structure.

15 (Original). The method of claim 10 including covering said first and second trenches with an insulating layer.

16 (Original). The method of claim 15 including covering said trenches with an insulating layer before exposing a metallization.

17 (Original). The method of claim 11 including spring biasing said tip against said structure using a cantilever.

18 (Original). The method of claim 17 including determining the position of said tip by reflecting a laser beam from said cantilever.

19 (Withdrawn). An atomic force microscopy tool comprising:

a cantilever to penetrate an integrated circuit;

a tip coupled to said cantilever; and

a circuit including a voltage source coupled between said tip and an integrated circuit.

20 (Withdrawn). The tool of claim 19 wherein said circuit includes an ammeter.

21 (Withdrawn). The tool of claim 19 wherein said circuit is connected to a metallization in said integrated circuit such that once the tip contacts said metallization, a short circuit is created.

22 (Withdrawn). The tool of claim 19 wherein an open circuit exists when said tool tip is electrically isolated from said metallization.